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Transfer of Pre-Assembled Block Copolymer Thin Film to Nanopattern Unconventional Substrates

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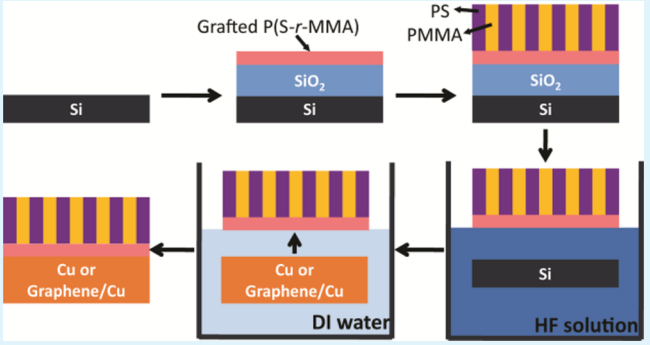
ABSTRACT: In this work, we demonstrate that a pre-assembled block copolymer (BCP) thin film can be floated, transferred, and utilized to effectively nanopattern unconventional substrates. As target substrates, we chose Cu foil and graphene/Cu foil since they cannot be nanopatterned via conventional processes due to the high surface roughness and susceptibility to harsh processing chemicals and etchants. Perpendicular hexagonal PMMA cylinder arrays in diblock copolymer poly(styrene-*block*-methyl methacrylate) [P(S-*b*-MMA)] thin films were preassembled on sacrificial SiO_2/Si substrates. The BCP thin film was floated at the air/water interface off of a SiO_2/Si substrate and then collected with the target substrate, leading to well-defined nanoporous PS templates on these uneven surfaces. We further show that the nanoporous template can be used for a subtractive process to fabricate nanoperforated graphene on Cu foil in sub-20 nm dimension, and for an additive process to create aluminum oxide nanodot arrays without any polymeric residues or use of harsh chemicals and etchants.



KEYWORDS: *block copolymer, lithography, unconventional substrates, graphene, floating*

INTRODUCTION

Pattern transferring from a self-assembled block copolymer (BCP) thin film to an underlying substrate, commonly referred to as BCP lithography,[1] is a useful nanopatterning method to create nanostructures for a range of applications from bit-patterned media,[2] quantum dot arrays,[3] memory device,[4] to micro- and nanoelectronics.[5,6] BCPs can self-assemble to create dense periodic arrays of nanodomains with exceptionally small feature sizes (sub-20 nm) over large-area with high fidelity. Compared to serial lithographic techniques such as ion-beam or electron-beam lithography the high throughput processing of BCPs' makes it appealing for large-scale nanofabrication.[7−9]

The past decade of work in this field has demonstrated successful pattern transfer from BCP templates to traditional substrates, typically oxides such as silicon oxide/silicon. The most commonly used method involves spin-coating a suitable BCP onto a chemically modified substrate, followed by thermal annealing to develop the morphology.[5] Other methods that are utilized to create self-assembled BCP templates include, but are not limited to, solvent annealing,[10] chemical guiding patterns,[11] roll casting,[12] and electric field induced alignment.[13] Once perpendicular domains of cylinders or lamellae are defined, selective removal of one of the domains results in a template that is used as a mask to pattern transfer into the underlying substrate. The success of these steps relies on (1) creation of a surface that is energetically nonpreferential to either polymer block,[14] (2) a very smooth substrate that minimizes film thickness variations,[15] and (3) tolerance of the substrate for patterning by wet or dry etchants.[16] However, the new emerging 2D materials for electronics,[17] nanofiltrations,[18] and nanostructured plasmonics,[19] these single atomic layered structures typically do not meet the aforementioned requirements, hence the process needs to be redefined.

For example, graphene is a two-dimensional sp^2-hybridized network of carbon atoms with a hexagonal structure and has emerged as a new material for ultrafast nanoelectronics,[17,20] transparent conductors,[21] and flexible electronics[22] due to its high charge mobility, potentially exceeding 200 000 $cm^2/(V{\cdot}s)$ at room temperature.[23] The challenge in patterning graphene comes from its sensitivity to standard plasma reactive ion etching (RIE) conditions, as well as standard wet processing reagents used in nanopatterning, which lead to a significant degradation in the electronic properties of graphene.[24−28] We recently reported the top-down fabrication of a graphene antidot lattice structure, called nanoperforated (NP) graphene, by using the cylinder-forming diblock copolymer poly(styrene-*block*-methyl methacrylate)[P(S-*b*-MMA)] as a BCP template.[29] However, isolating the NP graphene from processing materials was problematic, as it was sandwiched between two silicon oxide layers.[26,29] In addition, complete removal of polymeric residues left over from the pattern transfer by conventional organic solvents was difficult, as the BCP template was heavily cross-linked during the plasma RIE step.[26,30] These cross-linked residues typically require additional plasma

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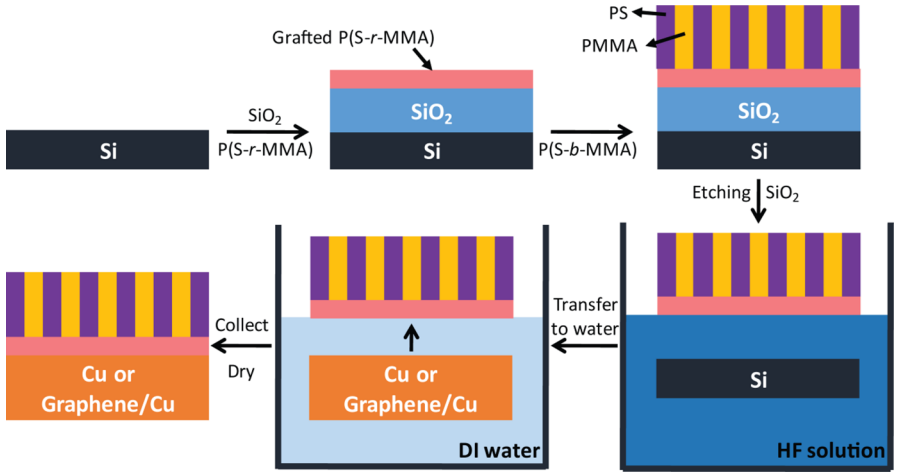
Scheme 1. Floating Transfer Process of a Pre-Assembled BCP Film to Cu Foil or Graphene/Cu Foil from a Sacrificial SiO_2/Si Substrate



etching, UV/ozone, or exposure to strong acids such as Piranha solution for complete removal.[16,31,32] However, these harsh processing steps inevitably result in the delamination or breaking of graphene from the substrate and often degrade its electronic properties, for example by reducing hole mobility and inducing unwanted doping effects.

In addition to a top-down approach for NP graphene, we also reported a bottom-up growth approach called barrier-guided chemical vapor deposition (BG-CVD).[33] By defining barriers of aluminum oxide (ALO) on the catalytic surface of Cu foil through BCP lithography, graphene growth was spatially controlled, growing only where the Cu was exposed on the surface. However, it was challenging to define this nanostructure on Cu foil using a typical direct self-assembly BCP approach because of the foil's highly textured surface and residual physical striations from its mechanical processing, resulting in undulations up to several hundreds of nanometers in height, making control of film thickness difficult by traditional spin-coating.[34] In addition, Cu foil is also easily damaged and oxidized by dry or wet etchants affecting its catalytic activity for graphene growth.[35,36] Therefore, in transferring a preassembled BCP film on Cu foil as a template for ALO barriers, graphene can be grown by BG-CVD.

In current literature, the ability to float polymer films off the substrate is known mainly to facilitate characterization. For example, Paeng et al. reported floating a thin film of polystyrene homopolymers from a mica substrate on to a TEM grid in order to examine segmental dynamics in the freestanding polymer thin film.[37] In the BCP literature, Zhang et al. utilized a P(S-*b*-MMA) template with 30 nm channels on a silicon wafer and floated the film by aqueous hydrofluoric acid onto a copper TEM grid.[38] The template-covered grid was then floated again onto an aqueous solution of PEO-covered CdSe nanorods to align them in the channels. In addition, Yang et al. demonstrated that a preassembled BCP film can be floated to be used as a nanoporous membrane.[39] To our knowledge, floated preassembled films have not yet been used to demonstrate pattern transfer onto an unconventional substrate.

To nanopattern unconventional substrates like Cu foil and graphene/Cu foil, we describe here in detail a method based on a simple floating transfer process using preassembled P(S-*b*-MMA) thin film on sacrificial substrates. Despite the inherent surface roughness of the substrates, excellent contact between the BCP and the substrate was achieved leading to densely packed perpendicular PMMA cylinders. In addition, the use of harsh etchants that can damage the substrate's surface were also avoided with this method. We demonstrate the versatility of this method through a subtractive as well as an additive process for the fabrication of NP graphene. In the subtractive process, we demonstrate that a floated BCP film on graphene/Cu substrate can be subjected to plasma RIE to create NP graphene. Raman spectroscopy and electron transport measurements confirmed that the resulting NP graphene is still mechanically intact and electronically conductive after all the processing steps. For the additive process, ALO nanodot arrays were fabricated directly on Cu foil. Upon lift-off of the PS template the exposed Cu surface was reported to maintain its catalytic activity.

EXPERIMENTAL SECTION

Graphene Synthesis via CVD. Cu foil (Alfa Aesar, product #13382) was loaded into a horizontal, 28 mm diameter quartz tube furnace, which was heated to 1050 °C under a 365 sccm flow of forming gas (95% Ar, 5% H_2). After annealing for 30 min, the temperature was reduced to 1030 °C, 24 ppm of CH_4 gas was introduced into the tube, and graphene was allowed to grow for 16 h, followed by quick cooling (~10 °C/s until below 700 °C).

Floating Transfer of BCP Thin Film to Cu Foil or Graphene/Cu Foil. 150 nm of SiO_2 was deposited on a silicon wafer by plasma-enhanced chemical vapor deposition (PlasmaTherm 70). A 1 wt % solution of hydroxyl terminated P(S-*r*-MMA) random copolymer (S: 70 mol%, MMA: 30 mol%) in toluene was spin-coated at 1000 rpm and annealed at 220 °C for 6 h under vacuum allowing the random copolymer to graft onto the SiO_2 surface. The annealed sample was washed with toluene to remove ungrafted random copolymers. 38 nm of P(S-*b*-MMA) (M_n(PS) = 46k, M_n(PMMA) = 21k, PDI = 1.09) (purchased from Polymer Source Inc., Dorval, Quebec, Canada) was spin-coated onto the random copolymer grafted SiO_2/Si, followed by annealing at 230 °C under vacuum for 3 h. The resulting BCP film was floated on the surface of 20 wt % hydrofluoric acid (HF) aqueous solution, and transferred to deionized (DI) water. The floated BCP film was transferred onto the preannealed Cu foil (detailed above) or graphene/Cu foil and dried for 24 h (Scheme 1).

Fabrication of NP Graphene—Subtractive Process. A transferred P(S-*b*-MMA) thin film on graphene/Cu foil was exposed to UV illumination (1000 mJ/cm^2) followed by dipping in acetic acid for 2 min and rinsing with DI water to selectively degrade and remove the PMMA cylinders. 20 W O_2 plasma RIE was utilized for various times to remove any residue inside the holes and to etch graphene. The

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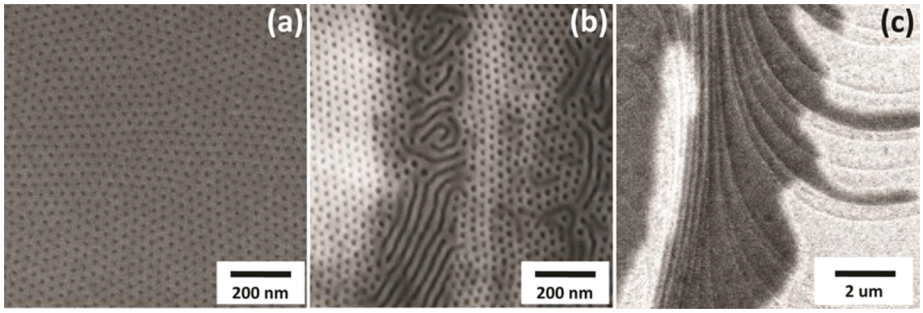

Figure 1. Top-down SEM images of assembled P(S-*b*-MMA) on (a) smooth surface of Si wafer, (b) rough surface of Cu foil, and (c) a zoomed out image of BCP on Cu foil. To induce perpendicular orientation of PMMA domain, a cross-linked P(S-*r*-MMA-*r*-GMA) layer was deposited on the top of both Si substrate and Cu foil.

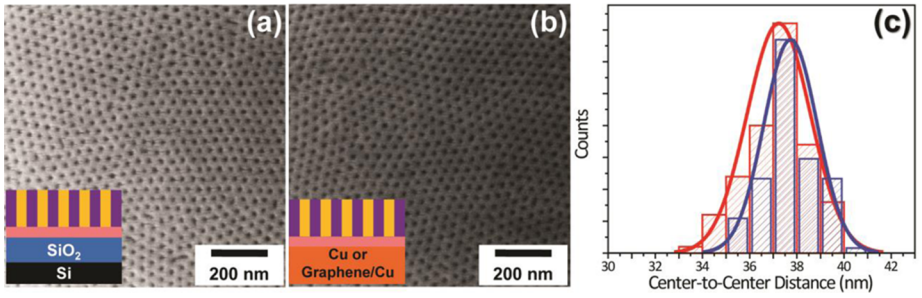

Figure 2. Top-down SEM images of (a) preassembled P(S-*b*-MMA) thin film on SiO_2/Si substrate, (b) transferred P(S-*b*-MMA) thin film on Cu foil, and (c) a histogram depicting the center-to-center distance, L_0, before the floating transfer process (red) and after (blue).

remaining PS template was removed by immersion in AZ-300T photoresist stripper at 80 °C for 20 min and further sonication at room temperature for 20 min.

Transfer of Graphene from Cu Foil to SiO_2/Si Substrate. Unpatterned or patterned graphene was transferred from Cu foil by spin-coating PMMA (950 PMMA 2C, Microchem Inc.) and etching Cu foil with an aqueous solution of 0.2 M HCl, 0.2 M $FeCl_3$. The PMMA/graphene film was washed by floating it on 1:9 HF (49%):DI water (v/v), subsequent floating on DI water, and allowed to dry on a 86 nm SiO_2/Si (p++) wafer. The PMMA was removed by immersing in boiling dichloromethane and the resulting sample was further washed with isopropyl alcohol.

ALO Nanodot Array Fabrication—Additive Process. Transferred P(S-*b*-MMA) thin film on Cu foil was exposed to ultraviolet (UV) illumination (1000 mJ/cm^2) to selectively degrade the PMMA cylinders. Degraded PMMA was removed by immersing the film in acetic acid for 2 min followed by rinsing with DI water. The substrate was then exposed to 20 W O_2 plasma RIE for 18 s and 10 nm of ALO was deposited through the PS template using an e-beam evaporation tool operating at <2 μtorr. Then, the remaining PS template and ALO on the top of PS were removed by immersion in commercial photoresist stripper (AZ-300T) at 80 °C for 20 min and further sonication at room temperature for 20 min.

Characterizations. Electron microscope images were acquired using LEO-1550 field-emission scanning electron microscopy (SEM) at 1−3 kV of accelerating voltage. Raman spectroscopy measurements were performed using Aramis Horiba Jobin Yvon Confocal Raman Microscope, with ∼1 μm^2 probing size at 633 nm excitation. The spectra were deconvoluted with Voigt function and peaks were identified. For electrical measurements, electrodes (50 nm Au) and a sacrificial mask (50 nm Cu) for the graphene channels were defined by thermal evaporation, utilizing a shadow mask. Exposed graphene was etched using a 50 W O_2 plasma RIE for 20 s, followed by selective removal of the sacrificial Cu mask in the Cu etchant, resulting in 15 × 120 μm (length × width) dimension of graphene transistors.

RESULTS AND DISCUSSION

Direct BCP Assembly on Cu Foil. The assembly of PMMA cylinders in P(S-*b*-MMA) on silicon (Figure 1a) and Cu foil (Figure 1b) by conventional spin-coating deposition showed stark differences in the morphology. The uneven surface of Cu foil (Figure 1c) prevented a uniform deposition of both the intermediate random copolymer layer, which is required for controlling the orientation of microdomains in P(S-*b*-MMA) thin film, and the BCP film. As the typical thickness of the nonpreferential layer is less than 10 nm and the BCP itself is less than 30 nm thick, the surface roughness of the Cu foil resulted in mixed morphology of parallel and perpendicular cylinders.

Floating Transfer of BCP Thin Film. To alleviate the problem of surface roughness and hence the nonuniform polymer deposition, we transferred to Cu foil a preassembled BCP film which was floated onto water surface. This method also facilitated the removal of the random copolymer layer between the BCP and the substrate, which is important as it eliminates any polymeric residues during the fabrication of NP graphene FETs. Typically, the hydroxyl terminated P(S-*r*-MMA) grafts onto the hydroxyl groups on the SiO_2 substrate.[14,40] Although this nonpreferential layer can be removed by wet or dry etchants, such as Piranha solution and O_2 plasma RIE, these conditions are too harsh to apply on Cu foil as the catalytic activity to grow single layer graphene is adversely affected. In the floating transfer method, HF essentially cleaves the Si−O bonds between the terminal hydroxyl group of P(S-*r*-MMA) and SiO_2, resulting in a freestanding film with intact preassembled BCP ready to be transferred.

The top-down SEM image of hexagonally packed perpendicular PMMA cylinders within PS matrix on a P(S-*r*-MMA)/SiO_2/Si (Figure 2a) substrate demonstrates the effectiveness of

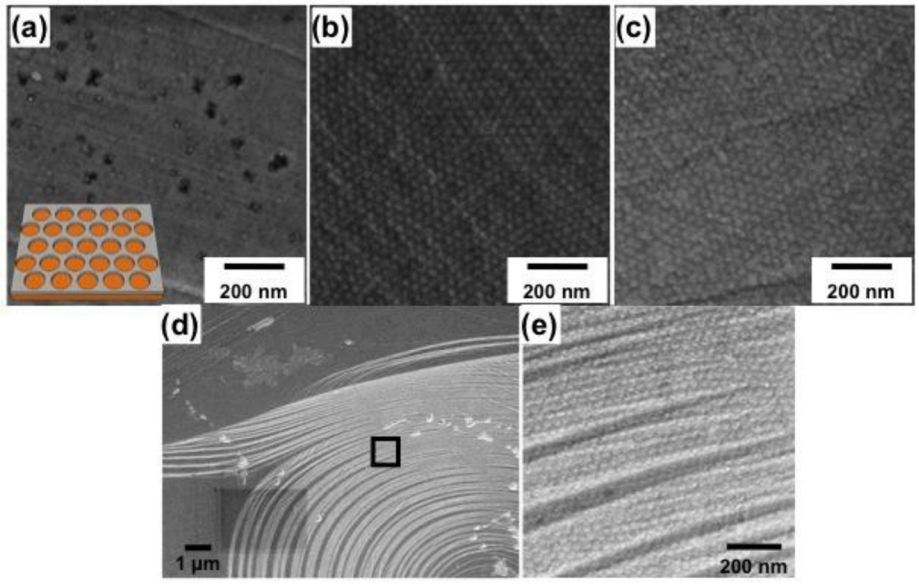

Figure 3. Top-down SEM images showing NP graphene on Cu foil fabricated by floating a preassembled BCP film onto graphene on Cu and then etching with O_2 plasma RIE generated with 20 W for (a) 25 s, (b) 35 s, and (c) 45 s. (d) SEM image showing the steps in graphene/Cu foil samples, and (e) magnified SEM image of black square region, showing defined NP structure persistent over the steps.

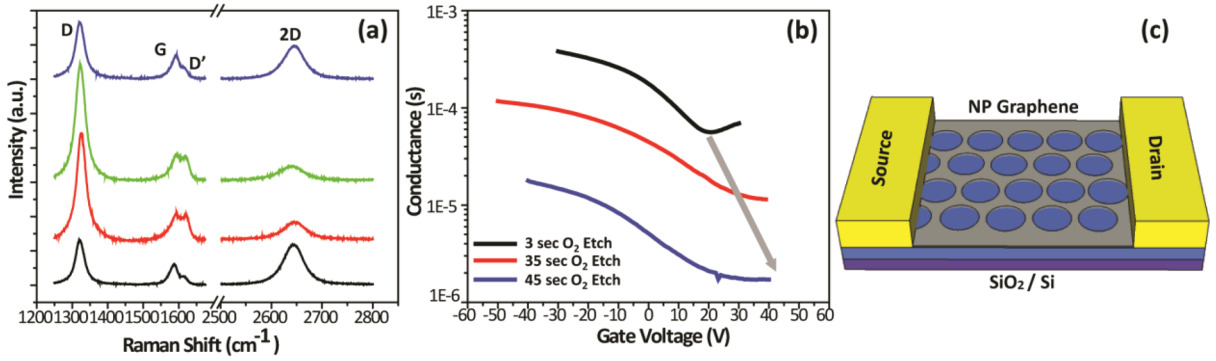

Figure 4. Physical and electrical characterization of NP graphene. (a) Raman scattering of NP graphene via etching with various 20 W O_2 plasma RIE times: 3 s (black), 35 s (red), 45 s (green), and 50 W for 3 s (blue). (b) Measured graphene conductance versus gate bias for NP graphene with various O_2 plasma RIE times: 3 s (black), 35 s (red), and 45 s (blue). (c) Schematic of NP graphene FET device.

this technique. This film was floated and transferred to Cu foil or graphene/Cu foil (Figure 2b). As evident from the SEM images and the histogram, both the periodicity (L_0 or center-to-center distance between PMMA domains) and the ordering of the domains were largely preserved after the floating transfer of the preassembled BCP film from the SiO_2/Si substrate to Cu foil or graphene/Cu foil.

Fabrication of NP Graphene on Cu Foil via a Subtractive Process. Generally, nanopatterning of graphene using BCP is performed on SiO_2/Si as it simplifies the fabrication of the field effect transistor (FET) devices and the Raman characterization.[26,29,41] However, after transferring graphene to SiO_2/Si, further processing becomes difficult due to the weak interactions between graphene and the substrate, hence isolated, large-area NP graphene is hard to fabricate. Most processes such as immersion in hot organic solvents with sonication, O_2 plasma RIE, and strong acids can all result in the destruction or oxidation of graphene. Conversely, when graphene is grown directly on Cu foil the strong interaction between the graphene and Cu atoms on the surface prevents any delamination or tearing of the nanopatterned graphene during the lift-off process. Figure 3 shows top-down SEM images of the resultant NP graphene via the floating transfer process of a preassembled BCP on graphene/Cu foil. Regardless of the surface roughness of Cu foil, after BCP lift-off, an antidot lattice was successfully transferred onto the graphene/Cu substrate.

In order to verify the successful pattern transfer of NP graphene, we characterized the samples using Raman spectroscopy (Figure 4a), which is a widely used nondestructive tool to probe the number of layers, doping behavior, and defects in graphene.[42,43] For characterization purposes, the resulting NP graphene on Cu foil were transferred to 89 nm thick thermal SiO_2/Si substrate by standard CVD graphene transfer method.[33]

Typically, pristine graphene on Si/SiO_2 shows two predominant characteristic peaks: G band at 1580−1590 cm^{-1} and 2D band at 2630−2640 cm^{-1}.[42,43] However, in NP graphene, we observed two additional peaks, D and D′ bands, at ∼1330 cm^{-1} and ∼1620 cm^{-1}, respectively.[26,44] The D and D′ bands were attributed to the disordered edges around the holes in the graphene lattice, which were formed by the O_2 plasma RIE pattern transfer with BCP templates.[26,29] The D band intensity increases with increasing 20 W O_2 plasma

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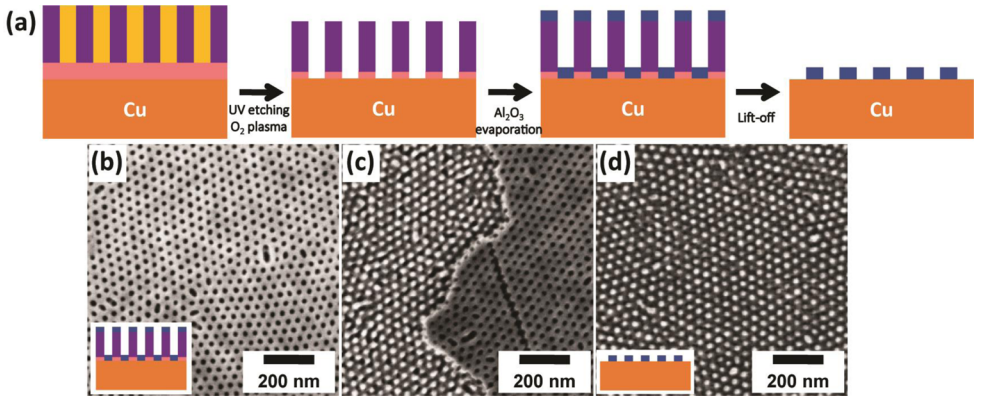

Figure 5. (a) Schematic depicting an additive process to fabricate ALO nanodot arrays on Cu foil using preassembled BCP films. Top-down SEM images of (b) PS matrix covered by ALO, (c) unsuccessful lift-off of ALO covered PS template with NMP, and (d) ALO nanodot arrays by successful lift-off with commercial photoresist stripper AZ300T.

etching times (Figure 4a, black, red, and green curves), as well as increasing plasma RIE power to 50 W (Figure 4a, blue curve).

Typically, the integrated intensity ratio of the D band to G band can be quantitatively correlated to the interdefect distance.[45,46] Since patterned graphene has disordered regions on the edges, this can be related to constriction width.[26,47] I_D/I_G values were found to be 2.36, 3.00, 3.64, and 2.54 for NP graphene prepared by 20 W O_2 plasma RIE for 3, 35, 45 s and by 50 W O_2 plasma for 3 s, respectively. Comparing these I_D/I_G values to the literature values (correlating I_D/I_G ratio to constriction width, w, we estimated a w of 15−20 nm.[26]

We further characterized the electrical properties of NP graphene in a FET device geometry at room temperature (Figure 4b). We defined electrodes on large-area NP graphene on SiO_2 (89 nm)/Si(p++) substrate, where SiO_2 acts as the back gate to modulate charge carrier density. In this geometry, unpatterned graphene typically exhibited ambipolar transport behavior with low ON/OFF conductance ratio of ∼5 and a mobility between 500−1000 $cm^2/V{\cdot}s$ at room temperature.[26,33] Upon nanopatterning with 20 W O_2 plasma for 3 s, the NP graphene device had a slight increase in its ON/OFF conductance ratio to ∼7 and decrease in mobility to ∼40 $cm^2/V{\cdot}s$. Further etching resulted in only a slight increase in the ON/OFF conductance ratio to ∼9. However, the mobility decreased significantly to 8 $cm^2/V{\cdot}s$ and 2 $cm^2/V{\cdot}s$ for 35 and 45 s etching times, respectively. In addition to the decreased mobility, the NP graphene devices demonstrated increased hole doping behavior as the Dirac point shifted from ∼20 V to >40 V. This induced hole doping is likely due to the exposure of oxygen plasma creating dangling bonds on the hole edges.[48] These results are consistent with our previous report where the increased O_2 plasma exposure causes degradation in mobility and increased hole doping in NP graphene devices.[26]

Fabrication of ALO Nanodot Arrays on Cu Foil via an Additive Process. The floated film was transferred onto the Cu substrate to directly grow NP graphene from the catalytic substrate. In our earlier paper,[33] we had described the device characteristics from this process, however the optimized conditions and details of the actual process used to float the BCP and establish the barrier arrays is described here. Figure 5a illustrates the fabrication of nanodot arrays of a barrier oxide, ALO, on Cu foil using the preassembled BCP film as a template. Once the BCP film was transferred to the Cu foil, the minority PMMA domains were degraded and ALO was deposited in the pores. The deposition was confirmed by the increased contrast in the top-down SEM image between the metal oxide/PS mask (bright) and the pores (dark) (Figure 5b). The lift-off process of the ALO covered PS template needed some optimization as the first attempt involved immersing the film in 80 °C *N*-methyl-2-pyrrolidone (NMP) (a conventional lift-off solvent) followed by sonication, which resulted in only partial lift-off (Figure 5c). The incomplete removal with NMP was partially due to the evaporated ALO covering the sidewalls of the PS template, thereby preventing proper contact of lift-off agents.[49−51] In addition, substantial cross-linking of the PS template by the O_2 plasma RIE treatment slowed down the swelling and complete lift-off of processing materials in common solvents.[26,30] To address this issue, two different methods have been examined in the literature, namely: (1) use of very strong oxidizing agents such as Piranha solution,[16] and (2) mild dry etching to remove metal on the top of PS template only.[50] While Piranha solution is effective in removing organic residues on various surfaces, it is not applicable to our work as Cu and graphene/Cu are readily oxidized by strong acids.[35] Alternatively, high power plasma can be utilized to etch ALO;[52] however, this process also creates the same effect of oxidizing the Cu surface and therefore, is not recommended for our purpose.

To resolve this issue, the commercial photoresist stripper AZ-300T,[53] consisting of NMP, 1,2-propanediol, and tetramethylammonium hydroxide (TMAH), was utilized for lift-off at moderate temperatures (80 °C) followed by sonication. Since the PS template covered with inorganic materials cannot be completely removed by normal organic solvent based processes, a stripping agent with a base and alcohol, in conjugation with sonication, is a simple and effective method to remove cross-linked PS template without lifting off the ALO dot arrays (Figure 5d). We had shown in our earlier paper[33] that with these preassembled patterns on the catalytic surface of Cu, single layer graphene can be grown by CVD around the ALO dots without the presence of carbon residues which can be converted to amorphous carbon at the elevated temperature.

CONCLUSIONS

We have developed a simple fabrication method using a P(S-*b*-MMA) template to nanopattern unconventional substrates such as Cu foil and graphene/Cu foil, which have high surface roughness and are easily damaged by various processing steps and reagents. Perpendicular hexagonal PMMA cylinder arrays

in a P(S-*b*-MMA) thin film were preassembled on sacrificial SiO_2/Si substrates. The thin film was floated at the air/water interface and then collected with the targeted substrates. A subtractive process was applied to graphene/Cu foil, yielding NP graphene where *w* was in sub-20 nm dimension. The versatility of this process was further demonstrated with an additive process to fabricate ALO nanodot arrays over large-area, which can be used for bottom-up synthesis of NP graphene via CVD. This process preserves the catalytic activity of the Cu foil. During these processes, we found an effective stripping agent to completely remove cross-linked polymeric residues without damaging the underlying graphene and substrate. The process developed here has the potential to increase the utility of BCP lithography for atypical substrates while maintaining substrate integrity, specifically in the field of catalysis, and graphene electronics.

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Author Contributions

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Notes

The authors declare no competing financial interest.

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ABBREVIATIONS

BCP, block copolymer; PMMA, poly(methyl methacrylate); P(S-*b*-MMA), poly(styrene-*block*-methyl methacrylate); BG-CVD, barrier-guided chemical vapor deposition; ALO, aluminum oxide; RIE, reactive ion etch; NP, nanoperforated

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